Jae-Hyun Lee

Assistant Professor
Dept. of Materials Science and Engineering
Ajou University

Address: Ajou University 206, Worldcup-Ro, Yeongtong-Gu Suwon 443-749, Korea
Mobile: (+82) (0)10-3065-4625, E-mail: skku02@gmail.com, nano.jhlee@gmail.com

Education

Ph.D Nano-Engineering	SKKU Advanced Institute of Nanotechnology (SAINT)	**Sungkyunkwan University**, Suwon, Korea Thesis: Synthesis and Application of Group-IV Semiconductor NWs, Graphene and its Hybrid Structures *Advisor : Prof. Dongmok Whang*	~ 2014.02 2009.03
B.S.	Materials Science and Engineering	**Sungkyunkwan University**, Suwon, Korea	~ 2009.02 2002.03

Work Experience

▪ **Ajou University,** Suwon, Korea -Dept. of Materials Science and Engineering	Assistant Professor	~ Present 2017.03
▪ **The University of Manchester**, *Manchester, UK.* - National Graphene Institute (NGI)	Researcher */Advisor: Prof. K. S. Novoselov* *2010 Nobel laureate*	~ 2017.02 2015.11
▪ **Sungkyunkwan University**, *Suwon, Korea* - SKKU Advanced Institute of Nanotechnology (SAINT)	Research Professor */Presidential Post-Doc. Fellow*	~ 2017.02 2014.11
▪ **Sungkyunkwan University**, *Suwon, Korea* - School of Advanced Material Science & Engineering	Post-Doc. */Advisor: Prof. Dongmok Whang*	~ 2014.10 2014.03
▪ **Samsung Advanced Institute of Technology**, *Korea* - Frontier Research Lab.	Research Intern	~ 2012.02 2011.03
▪ **Korea Army**, *Paju, Korea* - Artillery Fire Direction	Sergeant, Artillery man (Military service)	~ 2005.10 2003.10

Awards and Honors

▪ **Presidential Post-Doc. Fellowship**	NRF_Grant (₩150,000,000/year)	~2019.10 2014.11
▪ **Cheong-Am Science Fellowship**	POSCO T. J. Park Foundation	2014.10
▪ **2015 Dow Chemical Award in Korea**	Grand Prize	2015.04
▪ **The top 10 science and technology news of 2014**	The Korean Federation of S & T Societies (KOFST)	2014.12
▪ **BK21 Scholarship** - Korean Ministry of Education, Science and Technology		~ 2013 2009
▪ **Best Poster Award** - Nano Korea 2010		2010.08
▪ **Competition of Nanoscience and Technology** - Gwangju Institute of Science and Technology (GIST)	3rd prize	2008.11

Selected Publications

1. **J. H. Lee**, E. K. Lee, W. J. Joo, Y. Jang, B. S. Kim, J. Y. Lim, S. H. Choi, S. J. Ahn, J. R. Ahn, M. H. Park, C. W. Yang, B. L. Choi, S. W. Hwang, and D. Whang, "Wafer-scale growth of single-crystal monolayer graphene on reusable hydrogen-terminated germanium" ***Science*** 344, 286-289 (2014).
2. W. J. Joo******, **J. H. Lee****, Y. Jang, Y. N. Kwan, J. K. Jung, T. H. Kim, C. W. Yang, B. L. Choi, D. Whang, and S. W. Hwang, "Realization of Continuous 2D Zachariasen Graphene" ***Science Advances*** *3:e1601821* (2017*) (*: equal contribution)*
3. **J.-H. Lee**, S.-H. Choi, S. P. Patole, Y. Jang, K. Heo, W.-J. Joo, J.-B. Yoo, S. W. Hwang, and D. Whang, "Reliability Enhancement of Germanium Nanowires Using Graphene as a Protective Layer: Aspect of Thermal Stability" ***ACS Appl. Mater. Interfaces*** 4, 5069-5074 (2014).
4. **J. H. Lee**, M. S. Kim, J. Y. Lim, S. H. Jung, S. G. Kang, H. J. Shin, J. Y. Choi, S. W. Hwang, and D. Whang "CMOS-compatible catalytic growth of graphene on silicon dioxide substrate" ***Appl. Phys. Lett.*** 109, 053102 (2016).
5. **J. H. Lee**, B. S. Kim, S. H. Choi, Y. Jang, S. W. Hwang, and D. Whang, "A facile route to Si nanowire gate-all-around field effect transistors with a steep subthreshold slope" ***Nanoscale*** 5, 8968-8972 (2013).
6. N. H. Van******, **J. H. Lee****, D. Whang, and D. J. Kang "High-Performance CMOS Inverters Based on Axially Doped p- and n-type Regions on a Single Si Nanowire" ***Nanoscale*** 8, 12022-12028 (2016). (**: equal contribution*)

Full List of Publications

1. W. J. Joo******, **J. H. Lee****, Y. Jang, Y. N. Kwan, J. K. Jung, T. H. Kim, C. W. Yang, B. L. Choi, D. Whang, and S. W. Hwang, "Realization of Continuous 2D Zachariasen Graphene" ***Science Advances*** *3:e1601821* (2017*). (*: equal contribution)*
2. **J. H. Lee**, M. S. Kim, J. Y. Lim, S. H. Jung, S. G. Kang, H. J. Shin, J. Y. Choi, S. W. Hwang, and D. Whang "CMOS-compatible catalytic growth of graphene on silicon dioxide substrate" ***Appl. Phys. Lett.*** 109, 053102 (2016).
3. N. H. Van******, **J. H. Lee****, D. Whang, and D. J. Kang "Ultra-power complementary inverter circuits using axially doped p- and n-channel single Si nanowire field effect transistors" ***Nanoscale*** 8, 12022-12028 (2016). (**: equal contribution*)
4. J. E. Jin, **J. H. Lee**, J. H. Choi, H. K. Jang, J. Na, D. Whang, D. H. Kim, and G. T. Kim, "Catalytic etching of monolayer graphene at low temperature *via* carbon oxidation" ***Phys. Chem. Chem. Phys.*** 18, 101-109 (2016). *; selected as a back cover of the January (2016) issue of PCCP*
5. J. Y. Lim***, **J. H. Lee***, H. S. Jang, W. J. Joo, S. W. Hwang, and D. Whang, "Selective exfoliation of single layer graphene from non-uniform graphene grown on copper" ***Nanotechnology*** 26, 455304 (2015). (**: equal contribution*)
6. J. W. Lee, E. K. Lee, B. S. Kim, **J. H. Lee**, H. G. Kim, H. S. Jang, S. W. Hwang, B. L. Choi, and D. Whang "Thermoelectric Properties of Nanowires with Graphitic Shell" ***Chemsuschem*** 8, 2372-2377 (2015).
7. H. C. Shin, Y. Jang, T. H. Kim, J. H. Lee, D. H. Oh, S. J. Ahn, **J. H. Lee**, Y. K. Moon, J. H. Park, S. J. Yoo, C. Y Park, D. Whang. C. W. Yang, and J. R. Ahn, "Epitaxial Growth of a Single-Crystal Hybridized Boron Nitride and Graphene layer on a Wide-Band Gap Semiconductor Wafer" ***J. Am. Chem. Soc.*** 137, 6897-6905 (2015).
8. N. H. Van, **J. H. Lee**, D. Whang, and D. J. Kang, "Ultralow-power Non-volatile Memory Cells based on P(VDF-TrFE) Ferroelectric-gate CMOS Silicon Nanowire Channel Field-Effect Transistors" ***Nanoscale*** 7, 11660-11666 (2015).
9. N. H. Van, **J. H. Lee**, D. Whang, and D. J. Kang, "Low-Programmable-Voltage Nonvolatile Memory Devices Based on Omega-shaped Gate Organic Ferroelectric P(VDF-TrFE) Field Effect Transistors Using p-type Silicon Nanowire Channels" ***Nano-Micro Lett.*** 7, 35-41 (2015).
10. K. Heo, K. S. Cho, **J. H. Lee**, Y. Jang, S. Kim, S. W. Hwang, and D. Whang, "Physics-based modeling and

microwave characterization of graphene co-planar waveguides" ***Phys. Status Solidi - Rapid Res. Lett***. 8, 617-620 (2014).

11. **J.-H. Lee**, S.-H. Choi, S. P. Patole, Y. Jang, K. Heo, W.-J. Joo, J.-B. Yoo, S. W. Hwang, and D. Whang, "Reliability Enhancement of Germanium Nanowires Using Graphene as a Protective Layer: Aspect of Thermal Stability" ***ACS Appl. Mater. Interfaces*** 4, 5069-5074 (2014).
12. N. H. Van, **J. H. Lee**, J. I. Sohn, S. N. Cha, D. Whang, J. M. Kim, and D. J. Kang, "High performance Si nanowire field-effect-transistors based on a CMOS inverter with tunable threshold voltage" ***Nanoscale*** 6, 5479-5483 (2014).
13. **J. H. Lee**, E. K. Lee, W. J. Joo, Y. Jang, B. S. Kim, J. Y. Lim, S. H. Choi, S. J. Ahn, J. R. Ahn, M. H. Park, C. W. Yang, B. L. Choi, S. W. Hwang, and D. Whang, "Wafer-scale growth of single-crystal monolayer graphene on reusable hydrogen-terminated germanium" ***Science*** 344, 286-289 (2014).
    ; Featured by CNN, WSJ, Nanotechweb, Chemistry world, and domestic press.
    ; Selected as "**The top 10 science and technology news of 2014" KOFST**
14. N. H. Van, **J. H. Lee**, J. I. Sohn, S. Cha, D. Whang, J. M. Kim, and D. J. Kang, "Tunable threshold voltage of an n-type Si nanowire ferroelectric-gate field effect transistor for high-performance nonvolatile memory applications" ***Nanotechnology*** 25, 205201 (2014).
15. **J.-H. Lee**, Y. Jang, K. Heo, J.-M. Lee, S. H. Choi, W.-J. Joo, S. W. Hwang, and D. Whang, "Large-Scale Fabrication of 2-D Nanoporous Graphene Using a Thin Anodic Aluminum Oxide Etching Mask" ***J. Nanosci. Nanotechnol.*** 13, 7401-7405 (2013).
16. **J. H. Lee**, B. S. Kim, S. H. Choi, Y. Jang, S. W. Hwang, and D. Whang, "A facile route to Si nanowire gate-all-around field effect transistors with a steep subthreshold slope" ***Nanoscale*** 5, 8968-8972 (2013); Selected as this week "Hot article".
17. B. S. Kim, C. Xu, J. M. Lee, **J. H. Lee**, K. Son, S. W. Hwang, J. J. Park, and D. Whang, "Graphene shell on silica nanowires toward a nanostructured electrode with controlled morphology" ***Appl. Phys. Lett.*** 103, 013101 (2013); selected as a feature article of the July (2013) issue of APL
18. D. W. Kim, I. C. Nam, H. T. Kim, D. H. Hwang, M. G. Kang, B. H. Hong, S. J. Lee, **J. H. Lee**, D. Whang, and S. W. Hwang, "Real-time pulse measurement of nano-scale field effect transistors: Cancellation of displacement current and extraction of coupling capacitance" ***J. Nanosci. Nanotechnol.*** 13, 5513-5516 (2013).
19. C. S. Park, Y. Zhao, **J. H. Lee**, D. Whang, Y. Shon, Y. H. Song, and C. J. Lee, "Tunable bandgap of a single layer graphene doped by the manganese oxide using the electrochemical doping" ***Appl. Phys. Lett.*** 102, 032106 (2013).
20. M. S. Choi, D. J. Lee, S. J. Lee, D. H. Hwang, **J. H. Lee**, N. Aoki, Y. Ochiai, H. J. Kim, D. Whang, S. Kim, and S. W. Hwang, "Gate-dependent photoconductivity of single layer graphene grafted with metalloporphyrin molecules" ***Appl. Phys. Lett.*** 100, 032106 (2012).
21. B. S. Kim, **J. H. Lee**, K. Son, S. W. Hwang, B. L. Choi, E. K. Lee, and D. Whang, "Morphology control of self-catalyzed germanium nanostructures with graphitic carbon shell" ***J. Nanosci. Nanotechnol.*** 12, 4103-4107 (2012).
22. C. Xu, B. S. Kim, **J. H. Lee**, M. Kim, S. W. Hwang, B. L. Choi, E. K. Lee, J. M. Kim, and D. Whang, "Seed-free electrochemical growth of ZnO nanotube arrays on single-layer graphene" ***Mater. Lett.*** 72, 25-28 (2012).
23. J. E. Jin, **J. H. Lee**, D. H. Hwang, D. W. Kim, M. J. Kim, K. S. Son, D. Whang, and S. W. Hwang, "Graphene arch gate SiO_2 shell silicon nanowire core field effect transistors" ***Appl. Phys. Lett.*** 99, 212102 (2011).
24. B. S. Kim, **J. H. Lee**, K. Son, S. W. Hwang, B. L. Choi, E. K. Lee, J. M. Kim, and D. Whang, "Metastable $Ge_{1-x}C_x$ alloy nanowires" ***ACS Appl. Mater. Interfaces*** 4, 805-810 (2012).
25. T. W. Koo, D. S. Kim, **J. H. Lee**, Y. C. Jung, J. W. Lee, Y. S. Yu, S. W. Hwang, and D. Whang, "Axial p-n nanowire gated diodes as a direct probe of surface-dominated charge dynamics in semiconductor nanomaterials" ***J. Phys. Chem. C*** 115, 23552-23557 (2011).
26. C. Xu, **J. H. Lee**, J. C. Lee, B. S. Kim, S. W. Hwang, and D. Whang, "Electrochemical growth of vertically aligned ZnO nanorod arrays on oxidized bi-layer graphene electrode" ***CrystEngComm*** 13, 6036-6039 (2011).

27. J. S. Hwang, H. T. Kim, **J. H. Lee**, D. Whang, and S. W. Hwang, "Deoxyribonucleic acid sensitive graphene field-effect transistors" ***IEICE T. Electron.*** E94-C, 826-829 (2011).
28. C. Xu, T. W. Koo, B. S. Kim, **J. H. Lee**, S. W. Hwang, and D. Whang, "Large-scale solution-phase growth of Cu-doped ZnO nanowire networks" ***J. Nanosci. Nanotechnol.*** 11, 6062-6066 (2011).
29. J. Hong, K. Kim, N. Kwon, **J. Lee**, D. Whang, and I. Chung, "Fabrication of vertically aligned Si nanowires on Si (100) substrates utilizing metal-assisted etching" ***J. Vac. Sci. Technol. A*** 28, 735-740 (2010).
30. M. J. Song, J. H. Kim, S. K. Lee, **J. H. Lee**, D. S. Lim, S. W. Hwang, and D. Whang, "Pt-polyaniline nanocomposite on boron-doped diamond electrode for amperometic biosensor with low detection limit" ***Microchim. Acta*** 171, 249-255 (2010).
31. C. Yoon, K. Cho, **J. H. Lee**, D. Whang, B. M. Moon, and S. Kim, "P-type silicon nanowire-based nano-floating gate memory with Au nanoparticles embedded in Al_2O_3 gate layers" ***Solid State Sci.*** 12, 745-749 (2010).
32. J. H. Ahn, **J. H. Lee**, T. W. Koo, M. G. Kang, D. Whang, and S. W. Hwang, "Synthesis of small diameter silicon nanowires on SiO_2 and Si_3N_4 surfaces" ***IEICE T. Electron.*** E93-C, 546-551 (2010).
33. B. S. Kim, T. W. Koo, **J. H. Lee**, D. S. Kim, Y. C. Jung, S. W. Hwang, B. L. Choi, E. K. Lee, J. M. Kim, and D. Whang, "Catalyst-free growth of single-crystal silicon and germanium nanowires" ***Nano Lett.*** 9, 864-869 (2009).; Featured by domestic press.

Conference Presentations (Selected)

1. **J.H. Lee** "Growth of graphene on semiconductor nanomaterials" EKC 2016, Berlin, Germany (2016)
2. **J.H. Lee**, M. S. Kim, J. Y. Lim, S. H. Jung, S. Hwang, and D. Whang 'Ge vapor assisted catalytic growth of single layer graphene on silicon dioxide substrate" Pacific-Chem 2015, Hawaii, USA (2015)
3. **J. H. Lee**, W. J. Joo, S. W. Hwang and D. Whang "Growth of Single-Crystal Monolayer Graphene on H-Terminated Germanium Surface" MRS Fall Meeting, Boston, USA (2014)
4. **J. H. Lee** and D. Whang "Synthesizing Single Crystal Graphene on the Current Semiconductor Wafer Scale" Graphene World Summit 2014, Berkeley, USA (2014)
5. **J. H. Lee**, S. H. Choi, Y. Jang, S. W. Hwang and D. Whang "Realization of Single Si nanowire Gate All Around Field Effect Transistor Device" MRS Fall Meeting, Boston, USA (2013).
6. **J. H. Lee**, S. H. Choi, Y. M. Jang, B. S. Kim, S. W. Hwang and D. Whang "Reliability enhancement of Ge nanowire using graphene shell" E-MRS Fall Meeting, Warsaw, Poland (2012)
7. **J. H. Lee**, B. S. Kim, J. C. Lee, S. W. Hwang and D. Whang "Metal-catalyst free growth of graphene" E-MRS Spring Meeting, Strasbourg, France (2010)
8. **J. H. Lee**, T. W. Koo, J. W. Lee, B. S. Kim, S. W. Hwang and D. Whang "Large-scale synthesis of silicon nanowire by chemical vapor deposition" ISANN, Hawaii, USA (2009).

Conference Proceedings

1. D. W. Kim, H. T. Kim, D. H. Hwang, M. G. Kang, **J. H. Lee**, D. Whang, S. W. Hwang, Measurement of Femto-farad Gate Capacitance of a Silicon Nanowire FET Using Time-domain Pulse Response 2011 IEEE Nanotechnology Materials and Devices Conference.
2. J. S. Hwang, **J. H. Lee**, J. C. Lee, D. Whang, S. W. Hwang, Fabrication of graphene Field Effect Transistors by simple stripping from CVD grown Layers. Proceedings of 10th IEEE International conference on nanotechnology joint symposium with Nano Korea 2010

Patents_International

1. Method of Manufacturing Graphene by using Germanium layer. **US patent** (8,679,976) (2014)
2. Composite Structure of Graphene and Polymer and Method of Manufacturing the Same. **US patent** (9,172,022) (2015).
3. Graphene Ball Structure and Method of Manufacturing the Same. US patent application (13/681,955) (2012).
4. Wire structure and semiconductor device having the same, and method of manufacturing the wire structure.), US patent application (14/467,597) (2014)

Patents_Domestic

1. 게르마늄층을 이용한 그래핀 제조방법, 특허 출원(10-2010-0029509) (2010).
2. 그래핀 볼 구조체 및 그 제조방법, 특허 출원 (10-2011-0124398) (2011).
3. 그래핀과 폴리머의 복합체 및 그 제조방법. 특허 출원 (10-2011-0127863) (2011).
4. 나노와이어-그래핀 구조체, 이를 포함한 소자 및 그 제조방법. 특허 출원, (10-2012-01179110 (2012).
5. 그래핀 전사방법 및 이를 이용한 소자의 제조방법, 특허출원 (10-2012-0155320) (2012).
6. 와이어 구조체와 이를 구비하는 반도체 소자 및 와이어 구조체의 제조방법, 특허출원 (10-2013-0104508) (2013).
7. 그래핀 직성장 방법, 특허출원 (10-2015-0094005) (2015).
8. 대면적 단결정 2 차원 물질의 제조 방법, 특허 출원 (10-2015-0054239) (2015).